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ABSTRACT

This paper focuses on multimedia computer-based training programs on chip design. Their development must be fast and economical, in order to be affordable by technical university institutions. The self-produced teaching program Illusion, which demonstrates a monitor controller as an example of a small but complete chip design, was implemented to examine the optimization of development. A reference model is presented as a base for future implementations. It reduces implementation time to an acceptable amount. Also, the authors plan the VeriBox, a learning environment for the hardware description language VERILOG. (DDR)

Multimedia-Based Chip Design Education

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Abstract: Multimedia computer based training programs on chip design are at the center of this paper. Their development must be fast and economical, in order to be affordable by technical university institutions. The self-produced teaching program *Illusion*, demonstrating a monitor controller as an example of a small but complete chip design, was implemented to examine the optimization of development. As one result we present a *reference model* as a base for future implementations. It reduces implementation time to an acceptable amount. We plan the *VeriBox*, a learning environment for the hardware description language VERILOG.

Keywords: CBT, Multimedia, VLSI, Chip Design, Hardware Description Language

1 Introduction

In a time where more and more knowledge is required with its half-life decreasing [Hitzges et al. 94, 60], the classical teaching methods are too inflexible and time-consuming. The opportunities of the internet and the growing presence of household computers support knowledge acquisition independently of space and time, but increase the demands for new teaching methods and materials.

This paper deals with multimedia computer based training programs and animations, which are developed for teaching chip design at the Department of Integrated Circuit Design (E.I.S.) of the Technical University of Braunschweig, Germany. Our focus is the development and application of training programs in chip design *in addition* to the well-known teaching methods with lectures and labs. We produce computer based training programs (CBT) with authoring tools for image, sound, movement, and video, which are either presented in the lecture hall using notebook and projector, or are studied by students in parallel to the real practical hardware design in the class room or at home. For compact and time critical demonstrations, the results are also recorded on high-quality digital DV-CAM video.

As is well known, multimedia productions usually are quite time and cost intensive. We introduce the notion of *low-cost* and *low-time* searching for ways to produce CBTs for chip design with a reasonable amount of man power and time.

In the following, we begin with the self-developed teaching program demonstrating a monitor controller as an example of a small but complete chip design. We further study the pros and cons of a multimedia supplement of the classical education and chip design. We present a reference model as a frame for future projects. Finally we plan the project VeriBox offering an integrated learning environment for the hardware description language VERILOG. This includes the coupling of the learning program with a VERILOG simulator.

2 The Training Program Illusion – a Monitor Controller as a Complete Chip Design

Our development of the training program *Illusion* on the design of a simple monitor controller demonstrates many features of a complete chip design. This CBT was developed by several student theses with the authoring system Authorware 4.0 for Windows 95/98/NT. In the sections *Problem*, *Specification*, *HDL Model*, *Gate Model*, *FPGA Configuration*, and *Optimization*, a typical design flow is presented from the first idea via several abstraction levels to the complete circuit. The project is accompanied by a collection of exercises.

Section *Problem* presents the circuit to be developed, a monitor controller mapping image data from a memory to a video monitor. The functioning of such a monitor is presented in the second section *Specification*. It starts with a

short video for motivation. Lateron, active participation is supported by a simulation of the electron beam of a monitor.

Section *HDL Model* presents the register transfer model of the monitor controller in VERILOG underlining the importance of hardware description languages for simulation and synthesis. One module is studied in more detail and is constructed step by step. By suppressing less important information, the attention is focused. Additional information on the language syntax can be called on demand.

The linear organization of the CBT can be interrupted by an excursion to the real HDL model in a text editor. This model may be simulated and stimulated. Thus we bridge the training program with the real chip design tools. The student can apply his knowledge.

In the next section *Gate Model*, the manual and automatic translation of the RTL model into a gate model is animated and discussed. Real gate models are used, which were produced with the real-life gate library of a programmable chip. The student may analyze the circuit interactively (Fig. 1). The results are presented without having to use the cost intensive CAD tools restricted by licenses. This supports working at home.

As real simulations may take a long time, some test results already exist in the CBT. The simulation results before and after synthesis can be studied interactively.

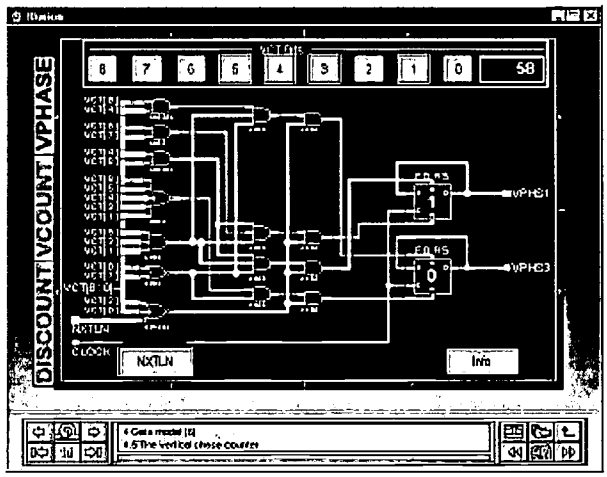

Figure 1: A screen of the CBT *Illusion*

The next section is on the *configuration* of a circuit on a programmable chip (FPGA). For motivation, the FPGA components can first be studied interactively, afterwards placement and routing is presented with animated and commented figures. The last section on *Optimization* is for advanced students on space minimization and speed increase.

In a separate section the student is challenged in a quiz where he can control the knowledge learned so far and receives feedback.

All sections are commented intensively by a female and a male speaker, such that not only the visual but also the audio senses are stimulated simultaneously (summation theory [FrLS97]). The inclusion of sound and speech has resulted in a significant increase of CBT design time, but has increased acceptance by the students.

By suitable standardization, we have tried to reduce this production disadvantage in the reference model discussed next.

3 A Reference Model Encapsulating our Experiences

After the production of four CBTs we tried to develop rules summarizing our experiences with the goal of decreasing future production costs. We noted that a significant amount of work is invested again and again in the design of the user interface, the navigation, and the subtleties and contradictions of programming in Authorware. This resulted in a reference model, which was used as a system of rules and frames in our following productions in the sense of low cost/low time. In addition to a unique user interface and navigation, basic rules for didactically founded layouts are mentioned and demonstrated explicitly [Schrei98; FrLS97].

The reference model is an Authorware application, whose source code is the base for any learning program. A copy of this frame is used and extended in further productions. The model is divided into protected areas, which must not be changed, and free areas, in which the programmer can implement his contents. The protected areas provide functions developed by us.

At the beginning, the student registers at the learning program by its name and comes via some opening credits to the main menu from which all sections can be reached. A section is divided into several pages. Each page is divided

into a presentation and a navigation area. The latter one includes elements for the local page control as well as the global control for the complete training program. In the middle of the navigation area, a bar indicates the progress within one section, and the present section and page title are indicated.

The global navigation contains of contents, a history list, and a bookmark list. The contents indicate sections and pages of the whole program. The history list shows the pages visited so far. By the bookmarks, pages can be marked for future sessions and stored with a remark. These pages can afterwards be directly selected just as from the contents list and the history list.

For several reasons we have chosen the resolution of the presentation window to be the VGA 640x480 pixels. This may appear old-fashioned, but when coupling the learning program with real chip design programs as described below, both windows can be shown on a high-resolution monitor. Moreover, we may use the advantage of a high quality digital video production system with an excellent recording quality.

Figure 2: A page of the reference model with some font examples

After negative experiences in applying the authoring tool Authorware we decided on the restriction to four frequent and always available fonts (Fig. 2). This avoids a later installation of fonts on the target systems and saves time in adapting our programs to differently configured systems. This restriction does not apply to fonts used in graphics.

In the sense of low cost/low time we have worked out rules standardizing the recording of spoken comments. This also applies to an even and good level control resulting in a satisfactory sound quality with acceptable effort.

4 VeriBox – A Training System for the Hardware Description Language VERILOG

Hardware description languages are at the center of chip design. VHDL and VERILOG are the two mainly used languages. We have decided on the language VERILOG and educate with professional tools such as Cadence VERILOG-XL and Synopsys Design-Compiler. While the basic concepts are developed in the lecture, the practical application of VERILOG in the exercises is meant to become more attractive and efficient by the CBT VeriBox.

The VeriBox includes the sections *Introduction*, *Basic Concepts*, *Examples and Exercises*, *Logic Synthesis*, and *Dictionary*. Interactivity of the VeriBox is a primary goal, by solving exercises and by executing simulations. Interactivity means a higher effort in the CBT production, but it increases the attractivity of the learning environment.

The *Introduction* gives an overview on hardware description languages and on differences and common features with conventional programming languages. A first example demonstrates the structure of VERILOG programs. Here an experienced programmer gets an intuitive imagination of the structure. Moreover, an introduction to the professional VERILOG simulator VERILOG-XL and the free PC version VeriWell is given. Thus the student is enabled to do the simulations at home.

In the *Basic Concepts*, important and difficult phenomena are trained such as parallelism and time, modularization and hierarchy, mixed mode models as well as behavior and structure. The multimedia presentation features turn out to be particularly applicable in the presentation of abstract phenomena. Together with audio comments, we have advantages as compared to printed media.

The module *Exercises and Examples* contains large VERILOG programs and contains links to all parts of the VeriBox. While we normally use small selected examples, these large VERILOG programs give a feeling of the complexity of the real-life model. These include a simple RISC processor, which is varied as a behavior model, a structure model, and a pipeline model.

The separate section *Logic Synthesis* distinguishes between synthesizable and non-synthesizable VERILOG constructs and discusses the implications of modeling styles on the synthesis results. In addition to theoretical considerations (Fig. 3), there is a multimedia introduction into the work with the Synopsys Design Compiler. By the parallel use of the learning program and the design compiler, a synthesis flow is demonstrated step by step and can be reproduced. If needed information on the different synthesis steps my be called. A synthesizable VERILOG model serves as an experimental input to the design compiler. Thus the learning program is not used independently, but is also used as a help in applying the real CAD tools.

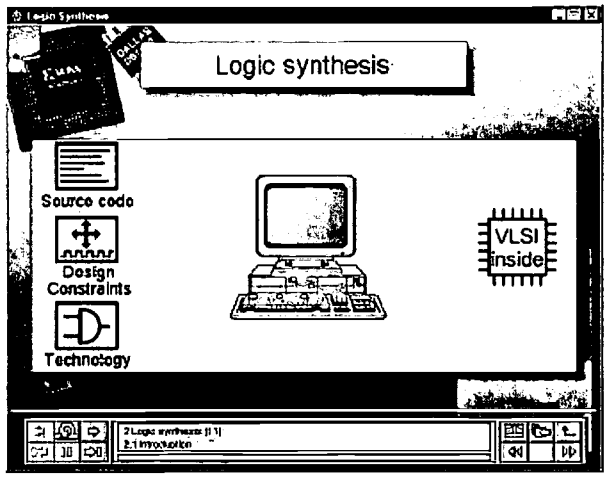

Figure 3: Example out of CBT logic synthesis

A focus of research in the development of the VeriBox is the search for suitable forms of interaction. To avoid the restriction of interaction to the turning of pages, we see the coupling of the CBT and professional CAD tools as a way of high-level interaction. Since the interface to the commercial chip design programs can be quite complex and are changing frequently, we strive for a *loose coupling* rather than a strong automatic coupling. By loose coupling we mean the simultaneous working with several programs at one monitor, where the data exchange is done by the student.

A typical application of the loose coupling is a problem presented by the learning program, which can only be solved by the use of a VERILOG simulator. The simulation result is than fed to the learning program by the student.

Another example of loose coupling is the *electronic tutor*. The student is led step by step through a professional tool by audio-visual instructions from the learning program. The synchronization is done by questions which the student can only answer from the actual position.

Another application will be the interactive manual. On demand, the program provides more detailed information and ways of application.

5 Summary and Outlook

Can "normal" technical institutions of a university afford to develop meaningful multimedia training programs? We have analyzed this question w.r.t. chip design as a part of technical computer science and have searched for cost efficient ways of implementation.

The application of our reference model has demonstrated in several projects that CBTs can be realized in the order of 12 weeks, even by beginners in this area. On the other hand, the CBT Illusion, which was developed without the reference model, has shown that multimedia productions can become quite time consuming. Thus multimedia productions require a large amount of time but can be handled in the frame of *low* cost/low time principles.

As a side effect there is the observation, that our project students had to deeply understand the technical matters to be presented in a CBT. We observed that motivation highly increases when developing own CBT programs. Thus students have understood the technical contents in a better way than in normal lectures or normal exercises.

Finally, universities profit from a large potential of students willing to invest their creativity. If this potential is guided by assistance, useful learning programs can be developed at affordable costs.

The real profit of the application of CBTs within chip design education remains to be analyzed in a long term application of the VeriBox and other CBTs.

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