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AUTHOR Reames, C. C.; Liu, M. T.
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ABSTRACT

An introduction to the problems of variable-length message transmission in distributed loop computer networks, with a summary of previous accomplishments in the area, begins this technically-oriented document. An improved technique, overcoming some of the inadequacies in presently used techniques, is proposed together with a conceptual model of its operation. The effects of the proposed technique, utilizing some of the properties of systems interfacing and hardware buffering, are discussed in terms of their action on message transmission. An appendix provides some possible hardware realizations of the model. (WDR)

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VARIABLE-LENGTH MESSAGE TRANSMISSION FOR DISTRIBUTED LOOP COMPUTER NETWORKS (Part I)

by

C. C. Reames and M. T. Liu

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The Computer and Information Science Research Center
The Ohio State University
Columbus, Ohio 43210

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ABSTRACT

An introduction to loop networks is given, with a summary of previous accomplishments in this area. The problems involved in the transmission of variable-length messages are outlined, and the present technique is shown to be inadequate. An improved variable-length message transmission scheme is proposed for distributed loop computer networks, and a conceptual model is developed of its operation. The model illustrates a method by which the nodal interface can delay incoming messages by hardware buffering just long enough for an outgoing message to be placed on the loop; advantage is taken of gaps between messages to clear out the delay buffer and to make room for future outgoing messages. The effects of the proposed technique on message transmission are discussed, and future research is mentioned. An appendix provides some possible hardware realizations of the model.

PREFACE

This report is the result of research supported in part by Grant Number GN 534.1 from the Office of Science Information Service, National Science Foundation to the Computer and Information Science Research Center, The Ohio State University.

The Computer and Information Science Research Center of The Ohio State University is an interdisciplinary research organization which consists of the staff, graduate students, and faculty of many University departments and laboratories. This report presents research accomplished in cooperation with the Department of Computer and Information Science.

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VARIABLE-LENGTH MESSAGE TRANSMISSION FOR DISTRIBUTED LOOP COMPUTER NETWORKS

Part I

I. INTRODUCTION

The importance of computer networking as a powerful national force is now being recognized both in the public and private sectors [8,23]. Several large networks are operating now and more are on their way [1,6]. Considerable interest has been shown recently in the design of distributed loop (ring) computer networks and switching systems. Such a network generally consists of a unidirectional digital communication channel, frequently based on the Bell T1 carrier system [9,14] or some of its derivatives [7], arranged as a closed loop or ring to which the nodes (which may be terminals, peripherals or processors) are connected through simple ring interfaces. Addressed blocks of data sent from a source node travel around the loop from interface to interface until the specified destination node is reached. The major advantages of a loop system are: 1) the ease of controling information, 2) the simplicity of message routing, 3) the low cost of initial construction, and 4) the low incremental cost for expansion.

Pioneering work was done at Bell Telephone Laboratories by Farmer and Newhall [13], who proposed and constructed a distributed loop switching system for bursty traffic. Pierce [21,22] extended the concept to include a hierarchy of interconnected loop systems. An experimental data block switching system has been implemented by Kropfl [20] with hardware and software provided by Coker [5]. Another experimental loop network is being designed and has been modeled by Hayes [16]. At the University of California, Irvine, Farber and his associates [10,11,12] are investigating an experimental Distributed Computer System (DCS). An experimental distributed loop network is also being developed by the National Security Agency [15] for future integration of its computer facilities. Even the National Weather Service [3,26] will use a loop system for its planned computer network.

A number of transmission control structures have been suggested by West [27] for use in loop systems, and a variety of them have been extensively investigated. Hayes and Sherman [17] studied the traffic and message delay in a single-loop system and, with Anderson [2], simulated the performance of loop systems. Traffic flow was also analyzed by Yuen *et al.* [28] and by Kaye [18]. Zafiropulo [29] has considered reliability of multi-loop systems. Spragins [25] has studied loops used for data collection and distribution, while Konheim [19] has treated the loop system as a priority service system. A summary of previous accomplishments and a unified model of computer communication systems has been presented by Chu and Konheim [4].

II. STATEMENT OF PROBLEM

With only a few exceptions, most loop systems studied or constructed have employed the concept of fixed-size frames (or slots) for message transmission. The reason for using a fixed-size frame is that message transmission protocol is thereby greatly simplified. The loop is initially filled with an integral number of empty frames, where a bit in the control field of each frame tells if that frame is empty (idle) or in use (busy). If a node has a message

it wishes to output which is shorter than the frame size, it simply waits for an empty frame to appear and then inserts its message into the frame; the unused frame space is wasted. Should the message be longer than the frame size, it must be broken into frame-size packets and transmitted one packet at a time. The disadvantages of this approach are the obvious ones of trying to fit variable-length messages into fixed-size frames.

A few attempts have been to provide loop systems for transmission of variable-length messages, but such systems have been severely handicapped by their inability to allow simultaneous use of the loop by several nodes. The distributed switching system of Farmer and Newhall [13] was such a variable-length message transmission system. It provided a control-passing mechanism which permitted only one node at a time to transmit a message onto the loop. This restriction, although highly undesirable, was also absolutely necessary; otherwise, two or more nodes transmitting onto the loop at the same time instant could interfere with each other. It is primarily for such reasons that most loop designs since that time have favored fixed-size frames over variable-length frames. Other factors being equal, however, use of variable-length frames could provide more efficient message transmission.

In this report, we propose an improved variable-length message transmission scheme which does not restrict use of the loop to just one node at a time. It puts variable-length message transmission on a par with currently used techniques for fixed-size packet transmission. Preliminary investigation by the authors [24] has established the feasibility of the proposed improvement; analytic and simulation studies are now underway to determine more about its properties and will be reported in Part II.

III. PROPOSAL FOR IMPROVED TRANSMISSION

To be efficient, any variable-length message transmission scheme must not restrict use of the loop to a single node at a time. It must ensure, however, that different messages, traveling around different portions of the loop, never meet and interfere with each other. That is equivalent to ensuring that a node which is in the process of transmitting a message out onto the loop will not at the same time receive an incoming message it must pass along to another node. But since we are assuming a distributed loop computer network, with each node acting independently and without knowledge of other nodes' actions, we cannot guarantee that such a situation will not occur.

A message store-and forward network like the ARPANET would handle the problem very easily by having each node buffer any incoming messages until transmission of an outgoing message was completed. That solution does not necessarily work for a distributed loop computer network, however, since the nodes may not be processors but may be unintelligent, unbuffered terminals and peripherals. The ring interface, which handles the actual loop message transmission for a node, is also a very simple device with little data buffering capability. That was done deliberately, to keep its cost low and its design simple. The ring interface, though, is the only place we could hope to do message buffering. But if the ring interface is to be expanded in capability to provide some degree of message buffering, it must be done carefully, without turning the interface into an expensive miniprocessor.

A technique for providing such a limited upgrade of the ring interface will now be presented. The method allows nodes to delay incoming messages by

hardware buffering just long enough for an outgoing message to be placed onto the loop. Advantage is taken of the gaps between incoming messages to clear out the delayed data, so as to make room for additional outgoing messages. The method has many desirable effects on message transmission, which will be discussed in Section V. First, however, a conceptual model of the message insertion and delaying technique will be developed to explain its operation. A sketch of possible hardware implementations is given in the appendix.

IV. DEVELOPMENT OF CONCEPTUAL MODEL

A representation of the message insertion and delaying technique proposed for the transmission of variable-length messages is shown in Figure 1. The model is a conceptual version of that part of the ring interface concerned with placing outgoing messages (from the attached node) onto the loop. Its primary component is an N-bit shift register (message delaying buffer) which shifts left once every clock pulse, thus transmitting one bit of data out onto the loop. The entire N-bit shift register is not shifted, but only the leftmost I bits of the shift register are activated at a given moment, where I is determined by the input selector. The input selector is responsible not only for activating the proper portion of the shift register but also for inserting the bits of incoming data into the shift register at bit position I. Thus the input data bits are always inserted, at each clock pulse, into the rightmost bit of the active portion of the shift register.

The other input to the shift register comes from the output buffer of the attached node. Thus the shift register must be at least as large as the node's output buffer (this size may vary from node to node), although if more buffering is desired, it can be several times larger. When the attached node has a message to output onto the loop, it places that message in its output buffer and requests the ring interface to send it. If enough space is currently available in the shift register, the output selector transfers the entire message into the inactive portion of the shift register (just to the right of bit I); if enough space is not available, the node must wait for more of the shift register to be cleared before transferring the message. After the message has been placed in the shift register, the interface then inspects the current incoming message (if any) and waits for the end of the incoming message to appear.

When the end of the current incoming message is detected (and regardless of what the next input may be), the input selector changes the point of insertion of additional incoming data to be the bit in the shift register just to the right of the rightmost bit of the output message already placed there. This change by the input selector also activates all the shift register to the left of this new point of insertion, thus causing the output message to be shifted out onto the loop ahead of any more incoming messages. Thus the shift register acts as a message delaying buffer for any additional incoming messages.

The input selector has another feature which allows the shift register to be eventually cleared of all delayed data. It has been described how the point of insertion of incoming data into the shift register (at bit position I) remains constant during the receipt of incoming messages, and how it increases when output messages are sent. But in addition, the input selector can also decrease the value of I (which represents a decrease in the amount of delayed data): during the gaps between the end of one incoming message and the beginning of the next, I is decremented by one at each clock pulse and the incoming

data are discarded (not stored in the shift register), until I becomes zero or an incoming message appears. The effect of this action is to eliminate the gaps between messages by replacing them with delayed data and to make room in the shift register for additional outgoing messages.

V. EFFECTS ON MESSAGE TRANSMISSION

The proposed technique of variable-length message transmission is expected to be a great improvement over the currently used method and could even be comparable to fixed-size frame transmission strategies. Any quantitative comparisons will have to be postponed until our analytic and simulation studies are completed, but certain qualitative observations can be made now.

1) The queueing delay a message waiting to get onto the loop may experience consists of two components. The delay prior to being transferred into the shift register depends on the size of the output message, the amount of data already being delayed, the size of the shift register, and the length and arrival rates of incoming messages. The subsequent delay prior to being output onto the loop is a function only of the remaining length of the current incoming message.

2) The transmission delay a message experiences in getting from the source to the destination node is equal to the sum of the delays experienced at each of the intermediate nodes. Each of these delays depends on the amount of data already delayed at a node when the message arrives there.

3) The total of the queueing and transmission delays experienced during message transmission is obviously a very complicated function of many parameters. Nevertheless, it is expected that on the average this total delay will be far less than that now imposed upon existing variable-length message transmission systems; it could even be less than in fixed-size frame transmission systems. Further analysis will be required to verify these expectations.

4) Since more than one node may output messages onto the loop at the same time instant, the utilization of the loop should be increased. Looking at it another way, for the same delay times the loop should be able to carry more traffic. For the same reason, the queueing delay should be less.

5) No frame space is ever wasted unless there is nothing to transmit over the loop. Frequently, there will be some delayed data in the shift register which can absorb the gaps between incoming messages. Similarly, a message is never delayed unless absolutely necessary and then only for the minimum time possible. These two factors working together should smooth out and stabilize traffic flow in the loop.

6) The rate at which a node can output messages onto the loop depends on how fast it can clear delayed data from its shift register. That depends on the overall system load and on the size and arrival rate of intermessage gaps. The latter are caused by lack of messages in a lightly loaded system or by receipt of a message by an upstream node. In short, the system provides automatic adjustment of message transmission rates which prevents one node from dominating the loop to the exclusion of all others.

7) The size of the shift register for a particular interface need be larger than the output buffer size of the attached node. Thus simple

devices, which have small output buffers, can also have small shift registers. The bigger the shift register is, however, the less is the chance that a sudden burst of output messages will find the shift register filled and will have to be queued. Thus a larger shift register serves to lessen the queueing delay and in effect can give certain nodes greater output priority than others.

VI. CONCLUSION

While it seems certain that the proposed upgrade of the ring interface will improve transmission of variable-length messages in a loop system and while all the above expectations seem reasonable and justified, proper verification requires that much more research be done. In that regard, study is now proceeding in the areas of analytic modeling and simulation. An analytic model of the queueing and transmission delays in the proposed system is the first research goal. In conjunction with that work, a simulation study of loop networks is being performed. Queueing and transmission delays for a variety of message distributions, traffic loads and transmission protocols will be investigated. These results will be reported in Part II.

There exists a large number of topics for further research in this area. Perhaps most interesting would be the extension of the results for single loop systems to hierarchies of interconnected loops. It is felt that variable-length message transmission schemes could play an important part in the development of regional and national distributed loop systems.

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APPENDIX: POSSIBLE HARDWARE IMPLEMENTATIONS

Figure 2 is a sketch of one possible hardware realization of the conceptual model (shown in Figure 1). In this particular implementation, we make the restrictions that 1) the shift register is only one bit larger than the output buffer and 2) the output buffer can thus be transferred into the shift register only when the shift register is cleared of all delayed data. The more general case will be treated in Part II. The design is modular in nature, so that the basic pattern can be repeated to form a shift register of any desired length.

In Figure 2 the Input Control Register serves as the Input Selector of the model. A "one" in a flip-flop of the Input Control Register activates the corresponding flip-flop in the Shift Register. The rightmost "one" of the Input Control Register causes the incoming data to be inserted into the corresponding flip-flop of the Shift Register.

Flip-flop M indicates the presence of an incoming message. When M is not set (between incoming messages), the Input Control Register is shifted left, deactivating more of the Shift Register. Flip-flop T indicates that a message has been transferred from the Output Buffer into the Shift Register; the transfer can occur only when the Shift Register is cleared of delayed data ($I_1 = 0$). If a transfer has taken place, then at the end of the current incoming message, all flip-flops of the Input Control Register are set to "one". This action activates all of the Shift Register and causes the output message to be shifted out onto the loop. Additional incoming messages will be inserted into the right end of the Shift Register and delayed there.

The Output Selector of the model is not needed in this restricted implementation and is replaced by a simple parallel transfer of the Output Buffer into the Shift Register. $Clock_1$ and $Clock_2$ are two timing signals derived from the bipolar format of the incoming data.

Other implementations are also possible using a random-access memory instead of the shift register design. Both linear and circular memory configurations have been considered. These implementations will be reported in Part II.

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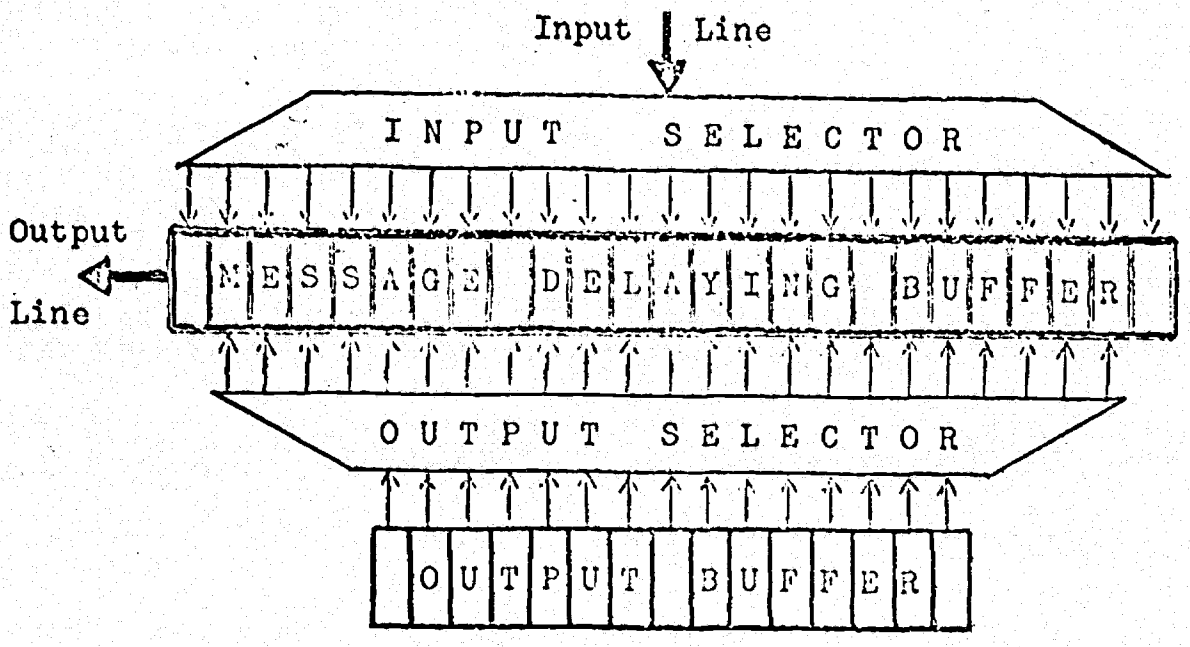

Figure 1. Conceptual Model

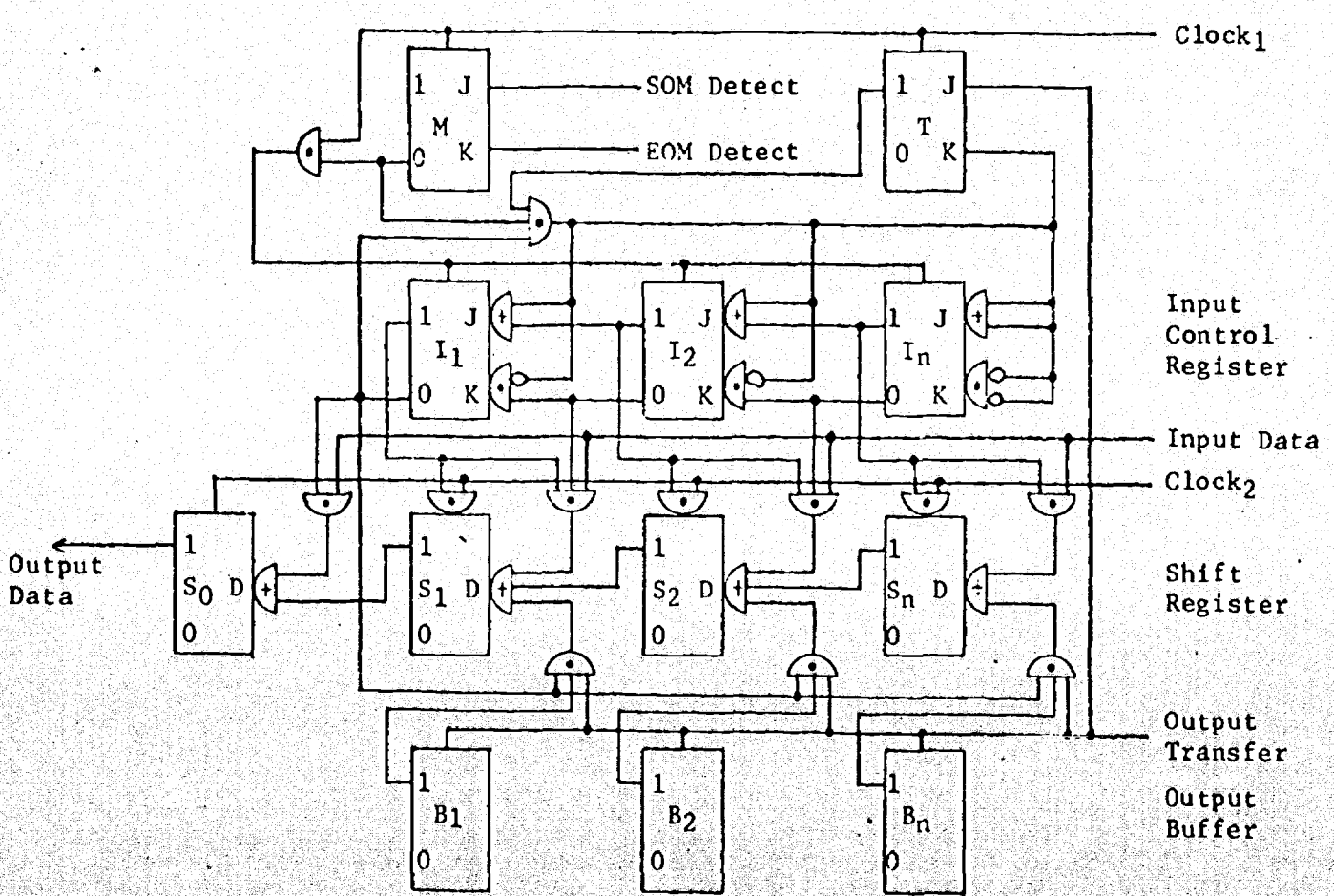

Figure 2. Shift Register Implementation